Amendments to the Claims:

Please amend Claims 1 and 3-6 and add new Claims 12-19 as follows:

1. (currently amended) An insulated gate device comprising a gate connected to a gate terminal and having a variable input capacitance means adjacent to ~~at~~ the gate terminal, said means comprising a variable capacitance such that as the device is switched between an off state and an on state, a ratio (C_{fiss}/C_{iiss}) between a final value of the capacitance (C_{fiss}) when the device is on and an initial value of the capacitance (C_{iiss}) when the device is off is ~~smaller than~~ $1 < C_{fiss}/C_{iiss} < 2.0$.

2. (original) A device as claimed in claim 1 comprising a power metal oxide silicon field effect transistor (MOSFET).

3. (currently amended) A device as claimed in claim 1 wherein said variable input capacitance means provides a capacitance such that the ratio (C_{fiss}/C_{iiss}) is ~~less than~~ $1 < C_{fiss}/C_{iiss} < 1.5$.

4. (currently amended) A device as claimed in claim 3 wherein said variable input capacitance means provides a capacitance such that the ratio is substantially equal to 1.

5. (currently amended) A device as claimed in claim 1, wherein said variable input capacitance means comprises ~~comprising~~ a capacitor ~~connected~~ between the gate terminal and the gate of the device.

6. (currently amended) A device as claimed in claim 2 wherein the MOSFET has a vertical structure in that the gate and a source of the device are provided on one face of a chip body of the device and a drain of the MOSFET is provided on an opposite face of the body, wherein said variable input capacitance means comprises a capacitor between the gate terminal and the gate of the device.

7. (original) A device as claimed in claim 6 wherein the capacitor is integrated on the chip body.

8. (original) A device as claimed in claim 7 wherein the capacitor is superimposed on the gate of the MOSFET.

9. (previously presented) A device as claimed in claim 5 wherein the capacitor is a discrete component connected in series between the gate and the gate terminal and packaged in the same package.

10. (previously presented) A device as claimed in claim 5 wherein the gate is connected directly to a fourth terminal of the device.

11. (original) A device as claimed in claim 9 wherein biasing resistors connected to the gate are included in the same package.

12. (new) A device as claimed in claim 1 wherein said variable input capacitance means comprises an insulation layer at the gate of the device.

13. (new) A device as claimed in claim 1 wherein said variable capacitance means is comprised in said gate.

14. (new) A device as claimed in claim 1 wherein said variable capacitance means is a device independent of said gate.

15. (new) An insulated gate device comprising a gate, the device having a capacitance at the gate, where a value of the capacitance is a function of an effective thickness of an insulation layer at the gate, the effective thickness of the insulation layer being selected to ensure that a first ratio between a final value of the capacitance when the device is on and an initial value of the capacitance when the device is off is smaller or equal to a second ratio of a maximum charge

receivable on the gate and a charge required to reach a threshold voltage of the gate of the device.

16. (new) An insulated gate device comprising a gate, the device having a capacitance at the gate, where a value of the capacitance is a function of an effective thickness of an insulation layer at the gate, the effective thickness of the insulation layer being selected to ensure that a first ratio between a final value of the capacitance when the device is on and an initial value of the capacitance when the device is off is smaller or equal to a second ratio of a maximum voltage applyable to the gate and a threshold voltage required on the gate to switch the device on.

17. (new) An insulated gate device comprising a gate and an insulation layer at the gate, the layer having an effective thickness (d) of at least a quotient of a device parameter and a ratio of maximum charge accommodatable on the gate and a minimum charge required on the gate for complete switching, minus one (1), the device parameter being equal to the product of an effective gate capacitance area (A) and a difference between an inverse of a first value of a gate capacitance of the insulated gate device, that is when the device is off and an inverse of a second value of the gate capacitance, that is when the device is on.

18. (new) A method of driving an insulated gate semiconductor device, the device comprising an insulation layer at a gate thereof providing a capacitance which varies between an initial value when the device is off and a final value when the device is on, the method comprising the step of depositing at least a Miller charge on the gate while the capacitance has said initial value.

19. (new) A method as claimed in claim 18 comprising the step of depositing substantially sufficient charge for a desired steady state switched on state of the device on the gate while the capacitance has said initial value.